REMARKS

No new matter has been added.

CONCLUSION

In view of the amendments set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on February 3, 2003.

John C Kennel — 2/3/03

Attorney for Applicant(s) — Date of Signature

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

The following is a "Marked Up" version showing the changes that the accompanying submission makes to the Claims of Application Serial No. 09/978,495:

In the Specification

The paragraph on page 5, lines 3 – 13 is changed as follows:

Fig. 1B is a timing diagram illustrating a three-signal group with delay provisioning. Signal 1 100, signal 2 105, and signal 3 110 are part of a three-signal group with signal 2 105 placed between signal 1 100 and signal 3 110. Whenever signals 100 and 105, or signals 105 and signal 110 switch simultaneously, in this particular example the three signals 100, 105, 110 are switching at time T1 115, a delay is performed by delay logic 120. Delay logic 120 provides a sufficient delay to signal 2 105 in order to prevent simultaneous switching with signal 1 100 and/or signal 3 110. Signal 2 105 switches at time T2 125. The delay is a **delay** d 130. Delay d 130 can be a predetermined period of time or any amount of time sufficient to prevent simultaneous switching with signal 2 105 and adjacent signal 1 100 and signal 3 110. The delay avoids any coupling interference in the event that signal 2 105 is an opposite switching signal to either signal 1 100 and/or signal 3 110.

The paragraph on page 6, lines 5 – 19 is changed as follows:

Fig. 1E is a timing diagram illustrating a five-signal group with an extended delay when **an** initial delay results in simultaneously switching with an adjacent signal. In this particular embodiment of the invention, signal 2 105 and signal 4 135 are never delayed, and always switch at their respective original switch times, in this example signal 2 105 switches at time T1 115 and

signal 4 135 switches at time T3 145. Signal 1 100, signal 3 110, and signal 5 140 switch at time T1 115, the same time that signal 2 105 switches. Delay logic 120 senses that adjacent signal 1 100 and signal 3 110 switch at the same time as signal 2 105, therefore a delay is provided to signal 1 100 and signal 3 110. Signal 1 100 now switches at time T3 145, the same time as signal 4 135, however the two signals are far enough removed from one another to avoid any coupling interference. Signal 3 110 would also be delayed to time T3 145, however, this condition would result in signal 3 110 switching at the same time as signal 4 135. Delay logic 120 therefore provides for signal 3 110 to be further delayed to time T5 155. The adjusted delayed timing diagram prevents adjacent signals from switching at the same times and avoids coupling interference when adjacent signals are switching opposite one another.

The paragraph on page 7, lines 7 – 14 is changed as follows:

Fig. 3 is a flow diagram illustrating transition of adjacent signals for a three signal group. Sensing and delay circuit 200 receives signals 100, 105, and 110, step 300. Signals 100 and 105 are sensed at the same time, step 305. Simultaneously, signals 105 and 110 are also sensed with one another at the same time, step 310. A determination is made if signals 100 and 105 are switching at the same time, step 315. A determination is also made whether signals 105 and 110 are switching at the same time, step 320. If the condition is **[true]** **"yes"** for either steps 315 or 320, then signal 2 105 is delayed, step 325. If steps 315 and 320 are both determined to be "no," then signal 2 105 is not delayed, step 330.

The paragraph beginning on page 7 line 15 and ending on page 8 line 3 is changed as follows:

Fig. 4 is a block diagram illustrating use of a sensing and delay circuit and buffers to transition a five-signal group. Buffer 400 is used for signal 1 100. Buffer 405 is used for signal 2 105. Buffer 410 is used for signal 3 110. Buffer 415 is used for signal 4 135. Buffer 420 is used for signal 5 140. Buffers 400, 410, and 420 are tri-state buffers that receive delay signals from sensing and delay circuit 425. A received delay signal to the respective buffer tri-states the respective signals. In this particular example delay signal 430 is provided to buffer 420. Delay signal 435 is provided to buffer 410. Delay signal 440 is provided to buffer 400. Sensing and delay circuit 425, in this embodiment, includes three separate circuit or logic blocks: sensing and delay circuit A 445; sensing and delay circuit B 450; and sensing and delay circuit **[A]** **C** 455. The respective sensing and delay circuits can include digital, analog, and/or combined circuits that sense and hold signals and trigger respective tri-state buffers 400, 405, 410, 415, and 420. In this particular embodiment, sensing and delay circuit A 445 senses signal 1 100 through sense signal 460 and signal 2 105 through sense signal 465. Sensing and delay circuit B 450 senses signal 2 105 through sense signal 470, signal 3 110 through sense signal 475, and signal 4 135 through sense signal 480. Sensing and delay circuit **[A]** **C** 455 senses signal 4 135 through sense signal 485 and signal 5 140 through sense signal 490. The use of sensing and delay circuit 425, in particular sensing and delay circuit 450 and tri-state buffer 410 to delay signal 3, provides a uninterrupted continuous delay. Delay signal 435 is provided to tri-state buffer 410 whenever the delay actually is required to take place. This prevents separate delay glitches that can cause aberrations in signal transmission.

In the Claims

46. (New) An apparatus comprising:

a circuit configured to detect a transition of a first signal and a transition of a second signal and provide a delay signal when the transitions of the first and the second signals occur simultaneously; and

a first buffer coupled to the circuit, wherein the first buffer is configured to delay the transition of the first signal in response to the delay signal.

47. (New) The apparatus of claim 46, wherein the first buffer is configured to delay the transition of the first signal until the transition of the second signal has completed.

48. (New) The apparatus of claim 46, wherein
the circuit is further configured to detect a transition of a third signal and provide the delay signal when the transitions of the first and third signals occur simultaneously.

49. (New) The apparatus of claim 48, wherein the first buffer is further configured to delay the transition of the first signal until the transition of the third signal has completed.

50. (New) The apparatus of claim 48 further comprising:
a second buffer configured to receive the second signal and provide a delayed second signal, wherein a delay of the second buffer is equal to an inherent delay of the first buffer; and
a third buffer configured to receive the third signal and provide a delayed third signal, wherein a delay of the third buffer is equal to the inherent delay of the first buffer.

51. (New) The apparatus of claim 50 wherein the first signal is adjacent to the second signal and the third signal.

52. (New) The apparatus of claim 50 further comprising:
a first sense signal, wherein the first signal is coupled to the circuit via the first sense signal;
a second sense signal, wherein the second signal is coupled to the circuit via the second sense signal; and
a third sense signal,wherein the third signal is coupled to the circuit via the third sense signal.

53. (New) The apparatus of claim 46 further comprising:
an integrated circuit coupled to the circuit.

54. (New) An apparatus comprising:
a circuit configured to detect a transition of each signal of a plurality of signals and provide a delay signal when any adjacent signals simultaneously transition; and
a plurality of buffers coupled to the circuit, wherein at least one buffer of the plurality is configured to delay at least one transition in response to the delay signal.

55. (New) The apparatus of claim 54, wherein the at least one buffer is configured to delay the at least one transition until all adjacent transitions to the at least one transition have completed.

56. (New) The apparatus of claim 54, further comprising:
a first circuit configured to detect a transition of a first signal and a transition of a second signal and provide a first delay signal when the transitions of the first and second signals occur simultaneously; and
a first buffer coupled to the first circuit, wherein the first buffer is configured to delay the transition of the first signal in response to the first delay signal.

57. (New) The apparatus of claim 56, wherein the first signal is adjacent to the second signal.

58. (New) The apparatus of claim 57, wherein in response to the first delay signal the first buffer is further configured to delay the transition of the first signal until the transition of the second signal has completed.

59. (New) The apparatus of claim 56, further comprising:
a second circuit configured to detect a transition of the second signal, a transition of a third signal, and a transition of a fourth signal and provide a second delay

signal when the transition of the third signal occurs simultaneously with at least one of the transition of the second signal and the transition of the fourth signal; and

a second buffer coupled to the second circuit, wherein the second buffer is configured to delay the transition of the third signal in response to the second delay signal.

60. (New) The apparatus of claim 59, wherein the third signal is adjacent to the second signal and the fourth signal.

61. (New) The apparatus of claim 59, wherein in response to the second delay signal the second buffer is further configured to delay the transition of the third signal until the transition of at least one of the third signal and the fourth signal has completed.

62. (New) The apparatus of claim 59, further comprising:

a third circuit configured to detect a transition of the fourth signal and a transition of a fifth signal and provide a third delay signal when the transitions of the fourth and fifth signals occur simultaneously; and

a third buffer coupled to the third circuit, wherein the third buffer is configured to delay the transition of the fifth signal in response to the third delay signal.

63. (New) The apparatus of claim 62, wherein the fourth signal is adjacent to the fifth signal.

64. (New) The apparatus of claim 62, wherein in response to the third delay signal the third buffer is further configured to delay the transition of the fifth signal until the transition of the fourth signal has completed.

65. (New) The apparatus of claim 62 further comprising:

a fourth buffer configured to receive the second signal and provide a delayed second signal, wherein a delay of the second buffer is equal to an inherent delay of the first buffer; and

a fifth buffer configured to receive the fourth signal and provide a delayed fourth signal, wherein a delay of the fifth buffer is equal to the inherent delay of the third buffer.

66. (New) The apparatus of claim 54, further comprising:

a second circuit configured to detect a transition of each signal of a second plurality of signals and provide a second delay signal when any adjacent signals simultaneously transition;

a second plurality of buffers coupled to the second circuit, wherein at least one buffer of the second plurality is configured to delay at least one transition in response to the second delay signal; and

a shield line between the plurality of signals and the second plurality of signals.